Predicting Microwave Digital Signal Integrity

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***Abstract*—High-speed digital signal integrity at data rates above 6 Gb/s is an obstacle to reliable serial link operation. Two signal integrity challenges include dispersion due to frequency-dependent losses and reflections created at impedance mismatches. Signal integrity analysis relies on time-domain simulation of pseudo-random data patterns. This paper explores a predictive method for interconnect eye closure caused by reflections at the transmitter and receiver and does not require extensive time domain simulation. Worst-case bounds on intersymbol interference and data-dependent jitter aid prediction for link budgets under channel variations. This method is applied to the design of a passive equalizer.**

***Index Terms*—Data dependent jitter, interconnect modeling, intersymbol interference, jitter, signal integrity.**

I. Introduction

DIGITAL signal integrity analysis is necessary for serial links operating over 6 Gb/s. Microwave digital signals propagating over interconnects are effected by loss, dispersion, and reflections that impair high-speed data recovery [1]. Higher data rates are demanded by high-performance memory requirements and high-density input/output (I/O) require high-speed links in compact packages [2]–[5]. A high-speed data eye, shown in Fig. 1, should remain open to accurately recover the received binary values in a range of channel scenarios. However, the eye diagram shown in this figure is significantly impacted by the channel response. Digital signal integrity characterizes the intersymbol interference (ISI) and data-dependent jitter (DDJ) that cause data eye closure. ISI and DDJ modeling is based on *a priori* knowledge of the channel step response [6]–[8] or lumped element models [9]. More recently, modeling work for jitter in channels with reflections has been proposed [10].

Signal integrity requires link budgeting based on empirical estimates for jitter generation and propagation through different electrical or optical blocks [11]. For instance, XAUI specifies peak deterministic jitter under 0.17 UI at the transmitter and 0.7 UI at the receiver [12]. However, predicting deterministic eye closure is complicated and many approaches rely on experimentally demonstrating ISI and DDJ. Unfortunately, the microwave channel environment suffers primarily from variability of one link to the next and depends on a large number of factors including the substrate material, packaging, and routing of signals. Therefore, optimization of link performance requires predictive modeling techniques for digital signal integrity that verify experimental results.

Above 6 Gb/s, ISI and DDJ result from a combination of low channel bandwidth and signal reflections. This paper provides an analytical method for estimating eye closure based on both of these impairments and is intended to limit the amount of time-domain simulation. A frequency-domain description of an impedance discontinuity characterizes the step response of the reflected signal [13]. The step response characteristics are directly related to eye height and width. Predicting signal integrity from the step response behavior can avoid extensive time-domain simulation subject to a pseudo-random bit sequence (PRBS) and determines signal integrity under channel variations.

In Section II, the fundamental trade-offs between broadband matching networks, referred to as passive equalizers, and reflections is discussed. Section III summarizes time-domain characterization of signal integrity based on the step response of the interconnect link. The step response analysis accounts for echoes caused by signal reflection in Section IV. The relationship between echoes and ISI and DDJ is developed in Section V and a method is presented for relating the impedance discontinuity, the signaling rate, and the distance between discontinuities (the interconnect length or delay) to digital signal integrity. Worst case and best case bounds are constructed. Finally, Section VI applies this algorithm to passive equalization. Passive equalizers, shown as a matching network in Fig. 1, have been shown to improve data rates and signal integrity with little power consumption and this work seeks to quantify the benefits of the equalizer.

II. Background: Matching Networks

Given a particular two-port matching network, Fano generalized Bode's earlier work by recognizing that an optimal matching network existed for a finite number of passive circuit elements [14], [15]. Matching networks are exploited in circuit design to maximize the gain-bandwidth product [16] and packaging bandwidth can be optimized with bondwire matching networks [17]. In interconnects, broadband behavior is generally desirable. Bode noted that a matching network, $Z(\omega)$, obeys

$$-\int_0^\infty \ln|\rho| d\omega \leq \frac{\pi}{Z_o C} \tag{1}$$

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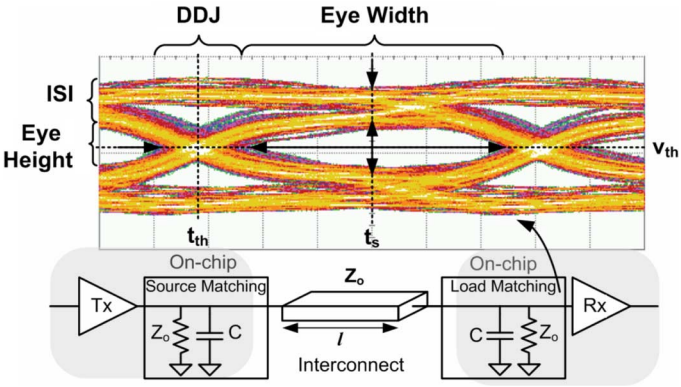

Fig. 1. Example of a high-speed interconnect with passive equalization networks for improved digital signal integrity with a 6 Gb/s data eye.

where is ρ the reflection coefficient between the matching network and the interconnect

$$Z_o = \lim_{\omega \to 0} \mathrm{Re}\{Z(\omega)\}$$
$$\omega C = \lim_{\omega \to \infty} \mathrm{Im}\left\{\frac{1}{Z(\omega)}\right\}. \quad (2)$$

In other words, the low-frequency channel impedance and high-frequency susceptance determine the achievable channel bandwidth. The limit in (1) exists for the product of the reflection coefficient and the bandwidth. In other words, increasing the tolerance for reflections increases the channel bandwidth. This insight motivates understanding the trade-off of bandwidth and reflection for digital signal integrity.

Consider a transmission line termination, Z_o, and capacitance, C. Approximating the integral in (1) with a bound on the acceptable reflection coefficient, $\rho_{\max} = (Z_o - Z)/(Z_o + Z)$, also bounds the bandwidth, BW

$$\mathrm{BW} \leq \frac{\pi}{Z_o C \ln\left|\frac{1}{\rho_{\max}}\right|}. \quad (3)$$

Impedance mismatch improves the bandwidth of the interconnect. However, the larger return loss reflects signal energy back to the transmitter. To improve the bandwidth, a two-port matching network, shown in Fig. 2, is constructed from an inductance–capacitance (*LC*) matching network that extends the 3 dB bandwidth of a 6 GHz channel, i.e., $\mathrm{BW} = 1/(\pi Z_o C)$. The interconnect is matched to the load impedance with one or more LC segments, where the C remains identical. The bandwidth of the $N = 2$ matching network is 50% greater. However, the return loss exceeds 5 dB from roughly 3–7 GHz and more signal reflection is anticipated.

Generally, a passive equalizer is a broadband matching network that is intended to improve the data eye with little power consumption. Several different passive equalizer topologies have been explored [7]. While a transfer function of the passive equalizer is straightforward to produce, a predictive signal integrity algorithm is needed to relate the matching network implementing the passive equalizer to digital signal integrity and verify the data eye improvement.

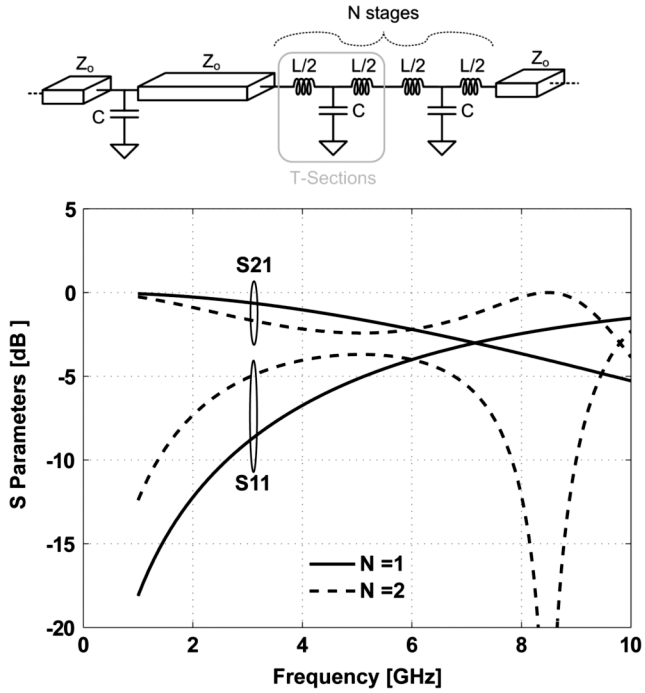

Fig. 2. Transmission and reflection *S*-parameters for lumped matching networks.

III. Time Domain Characterization

Digital signal integrity is related to the interconnect step response. The approach presented in this paper attempts to characterize the step response at an impedance mismatch to make signal integrity predictions. Signal reflections impact the step response and cause intersymbol interference (ISI) and data-dependent jitter (DDJ). Assuming a linear channel response, the received digital signal is

$$r(t) = \sum_{n=-\infty}^{0} a_n[s(t - nT) - s(t - (n+1)T)] \quad (4)$$

where a_n is the symbol value, $s(t)$ is a input step response, and T is the symbol period. In this work, the symbol value represents a general pulse-amplitude modulation scheme. The received step consists of a bandwidth-limited step response, $s_r(t)$, and reflections, $v_{r,k}(t)$

$$s(t) = s_r(t) + \sum_{k=1}^{\infty} v_{r,k}(t - 2kT_d), \quad (5)$$

where T_d is the interconnect delay. Fig. 3 illustrates the step response described in (5). Initially, the step arrives at the load and takes t_{th} seconds to arrive at the nominal threshold voltage, v_{th}; by definition $s_r(t_{\mathrm{th}}) = v_{\mathrm{th}}$. The optimal sampling time, t_s, is assumed to occur $T/2$ seconds after t_{th}. Then, the kth echo arrives back at the load after $2kT_d$ seconds. During this interval, n_k symbols are subsequently transmitted. The kth reflection arrives

$$n_k = \lfloor (t_s - 2kT_d)/T \rfloor \quad (6)$$

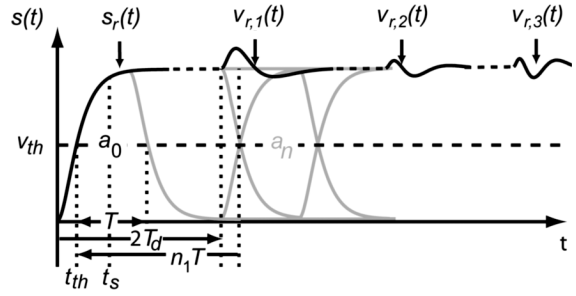

Fig. 3. Step response at load over several echoes.

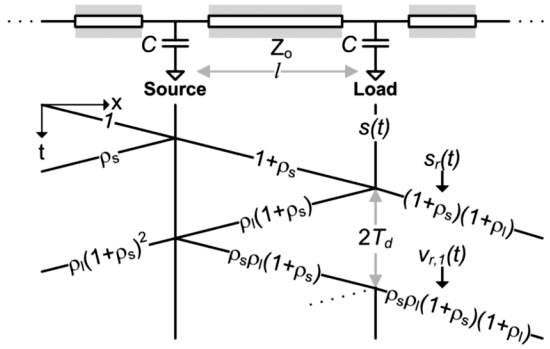

Fig. 4. Graphical representation of reflections between source and load.

symbols where $\lfloor\rfloor$ rounds down to the nearest integer. The phase velocity, v_p, of the signal relates the delay to the interconnect length

$$l = v_p T_d. \tag{7}$$

Accordingly, reflections become an issue for lengths exceeding roughly 1 cm at 10 Gb/s. Presumably, reflections take more than one symbol period to propagate along the transmission line and reflection generated ISI compounds other sources of ISI such as reduced bandwidth. A receiver (load) echo requires reflections at both the receiver and the transmitter (source). Substituting (5) into (4), the received signal is

$$r(t) = \sum_{n=-\infty}^{0} a_n[s_r(t-nT) - s_r(t-(n+1)T)] + v_{\text{echo}}(t)$$

where

$$v_{\text{echo}}(t) = \sum_{n=-\infty}^{-1} \Delta a_n \sum_{k=1}^{\infty} v_{r,k}(t - nT - 2kT_d). \tag{8}$$

The first term in $r(t)$ is the filtered (bandwidth-limited) symbol response and bandwidth-limited ISI. The second term is the echo of prior symbols, henceforth referred to as echo ISI. The symbols, a_n, are translated to a difference between consecutive symbols, $\Delta a_n = a_n - a_{n+1}$. For NRZ signals, $\Delta a_n \in \{-1, 0, 1\}$, maps consecutive symbols to rising or falling transitions. Therefore, Δa_n must alternate between the values of -1 and 1 with a random number of interposing 0s.

IV. Step Response Reflections in Transmission Lines

The signal decomposition in (5) isolates the undesirable contributions to signal integrity. Fig. 4 illustrates the generation of echoes due to source and load impedance discontinuities. While the following discussion treats a single pair of source and load impedance discontinuities, the results can be extended to handle additional discontinuities. Impedance mismatch generally reflects high-frequency signal components. Therefore, the rise/fall time of the step response decreases and the signal swing at the sampling point is reduced. From Fig. 4, the step response at the load is

$$s(t) = e^{-\alpha l} L^{-1}\left\{\sum_{k=0}^{\infty} \rho_s^k \rho_l^k e^{-2(\alpha+j\beta)kl}(1+\rho_s)(1+\rho_l)\frac{1}{s}\right\} \tag{9}$$

where ρ_s and ρ_l are respectively the reflection coefficients at the source and load, α and β are the attenuation and phase constants, and $L^{-1}\{\}$ is the inverse Laplace transform. The reflection coefficient is generally a frequency domain characterization and the inverse Laplace transform generates the time-domain step response required in (8). The attenuation constant is assumed to be frequency independent to factor it from the step response and the echoes. The $1/s$ term is the ideal unit step generated at the source and could be more realistically treated with finite rise time [19]. Given the matching network, the frequency response for the reflection coefficients allows a solution to (9) and, hence, (8). From (9), the bandwidth-limited step response, $s_r(t)$, is found for $k = 0$, and echoes, $v_{r,k}(t)$, are found for positive values of k. The bandwidth-limited step and echoes are

$$\begin{aligned} s_r(t) &= e^{-\alpha l} L^{-1}\left\{\frac{(1+\rho_s)(1+\rho_l)}{s}\right\} \\ v_{r,k}(t) &= e^{-\alpha(2k+1)l} e^{-j2kT_d} \\ &\quad \times L^{-1}\left\{\rho_s^k \rho_l^k \frac{(1+\rho_s)(1+\rho_l)}{s}\right\}. \end{aligned} \tag{10}$$

If the response in the transforms of (10) can be determined, the signal integrity can be predicted. Since the attenuation and delay are prefactors in (10), they can be handled subsequently. Attenuation impacts the step response but more strongly reduces the echoes due to the multiple trips along the interconnect. Ignoring attenuation provides worst case bounds on the ISI and DDJ for a signal integrity link budget. For short, low-loss interconnects, attenuation tends to be low and does not diminish reflections significantly, causing echo ISI. However, longer interconnects have more attenuation and bandwidth-limited ISI may dominate the echo ISI. Frequency-dependent attenuation of the lossy interconnect also tends to reduce the impact of echoes.

In the following sections, the reflected signal behavior is derived from the inverse Laplace transforms in (10). The discussion specifically studies a pair of shunt capacitances to derive practical bounds and offers a generalized approach to relating the impedance mismatches to reflections with a chain (ABCD) matrix description.

A. Reflections due to Shunt Capacitance

Shunt capacitances occur at output drivers, chip-to-board bonds, closely routed wires, and connectors. Given a pair of parallel resistance–capacitance (*RC*) terminations at the source

TABLE I
REFLECTION COEFFICIENTS, $A_{k,j}$, DUE TO SHUNT CAPACITANCE DISCONTINUITIES

k \ j	1	2	3	4	5	6	7
1^{st}	0	1/2	-1/6	0	0	0	0
2^{nd}	0	1/2	-1/2	1/8	-1/120	0	0
3^{rd}	0	1/2	-5/6	5/12	-1/12	1/144	-1/5040

and load (similar to the discussed in Section II), the reflection coefficient is

$$\rho = \frac{Z_L - Z_o}{Z_L + Z_o} = \frac{-sC}{\frac{2}{Z_o} + sC} = \frac{-s\tau}{1 + s\tau}$$

where

$$\tau = \frac{Z_o C}{2}. \tag{11}$$

Here, the reflection coefficient has been characterized as a time constant, τ. If the source and load capacitances are identical, reflection coefficients are identical assuming the discontinuities are widely separated. The step response behavior subject to this first-order reflection coefficient is found by substituting (11) into (10). At the load, the filtered step response is

$$s_r(t) = 1 - (1 + (t/\tau))e^{-t/\tau}. \tag{12}$$

The filtered step response reaches $v_{\rm th} = 0.5$ at $t_{\rm th} = 1.7\tau$. The kth echo is

$$v_{r,k}(t) = \sum_{j=0}^{2k+1} A_{k,j}(t/\tau)^j e^{-t/\tau} \tag{13}$$

where the coefficient, $A_{k,j}$, is defined in Table I. Closed-form values for the coefficients are given in [10]. These values only apply to a pair of identical shunt capacitances but can be determined for other combinations of impedance discontinuities.

The load echoes are plotted in Fig. 5 and normalized to time constant, τ. The first echo is largest in amplitude and each subsequent echo is weaker. Interestingly, the duration of the echoes does not change dramatically. From (13), the first echo is

$$v_{r,1}(t) = \left(\frac{(t/\tau)^2}{2} - \frac{(t/\tau)^3}{6}\right) e^{-t/\tau} \tag{14}$$

for which the maximum and minimum reflected values are

$$v_{r,\max} = 0.13 \quad v_{r,\min} = -0.057 \tag{15}$$

and occur at

$$t_{\max} = (3 - \sqrt{3})\tau \approx 1.27\tau$$
$$t_{\min} = (3 + \sqrt{3})\tau \approx 4.73\tau. \tag{16}$$

From (16), the reflected voltage extrema are separated by 3.5τ, or roughly 86 ps if $\tau = 25$ ps. Interestingly, the voltage extrema are independent of τ but the interval between maximum and minimum extrema will depend on τ. Moreover, each reflection

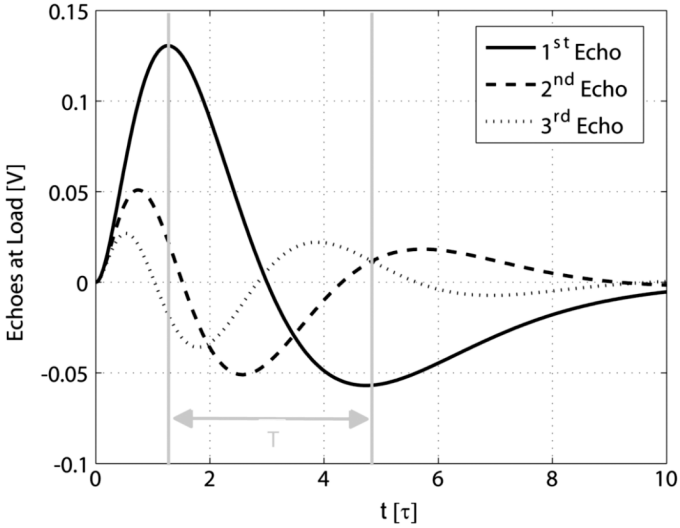

Fig. 5. The load echoes caused by a pair of shunt capacitances at the source and load.

in Fig. 5 lasts more than 8τ. Therefore, a 10 Gb/s signal would be subject to a single reflection over two symbol intervals. This observation is accounted for in subsequent discussions of the relationship between signal integrity and echoes.

B. Reflections Due to a General Discontinuity

A general two port matching network such as a passive equalizer may be used to improve the signal integrity and mitigate ISI. The two port network is generally expressed as a chain matrix that relates the voltage and current at the input port (port 1) and output port (port 2) [20].

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \boldsymbol{T} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}. \tag{17}$$

For a lumped series-L, shunt-C network the matrix is

$$\boldsymbol{T} = \boldsymbol{T}_L \boldsymbol{T}_C = \begin{bmatrix} 1 & sL \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC & 1 \end{bmatrix} = \begin{bmatrix} s^2\mathrm{LC} & sL \\ sC & 1 \end{bmatrix}. \tag{18}$$

The chain matrix translates into *S*-parameters according to

$$S_{11} = \frac{AZ_{ol} + B - CZ_{os}^* Z_{ol} - DZ_{os}^*}{AZ_{ol} + B + CZ_{os}Z_{ol} + DZ_{os}}$$
$$S_{21} = \frac{2}{AZ_{ol} + B + CZ_{os}Z_{ol} + DZ_{os}} \tag{19}$$

where complex source and load impedances, Z_{os} and Z_{ol}, terminate the interconnect and the superscript, $*$, denotes the complex conjugate [21]. Finally, the reflection coefficient looking into the network is

$$\rho_M = S_{11} + \frac{\rho_l S_{12} S_{21}}{1 - S_{22}\rho_l}. \tag{20}$$

S11 is equal to the reflection coefficient only if the load reflection coefficient is zero. The reflections are found by substituting

(20) into (10). Therefore, the echo that results from any arbitrary source and load matching network is determined.

V. Digital Signal Integrity

Characterizing the eye closure in the voltage and time domains is possible given the filtered step and echo response. In the first part of this section, the step response is related to bandwidth-limited ISI and DDJ. In the second part of this section, the reflections are related to the echo ISI and DDJ. Eye closure for an interconnect limited by source and load shunt capacitance provides an example to find bounds on the ISI and DDJ.

A. Bandwidth-Limited ISI

The step response, $s_r(t)$, has a reduced rise and fall transition time that spreads signal energy over neighboring symbols. The bandwidth-limited peak ISI is

$$\mathrm{ISI}(t_s) = \sum_{n=-\infty}^{-1} |v_s - s_r(t_s - nT)|$$

where

$$\lim_{t\to\infty} s_r(t) = v_s. \tag{21}$$

The bandwidth-limited ISI is the residual deviation of the step response from the voltage swing at symbol intervals from the sampling time of the current symbol. The eye height is the difference between the minimum voltage associated with the logical value of one and the maximum voltage associated with the logical value of zero at the sampling point

$$\mathrm{Height}(t_s) = 2[s_r(t_s) - \mathrm{ISI}(t_s)] - v_s. \tag{22}$$

The first term in (22) accounts for the step response at the desired symbol while the second term is the peak ISI caused by the residual deviation at the sampling point. The sampling point occurs roughly $T/2$ seconds after the threshold crossing time in most instances, i.e., $t_s = t_{\mathrm{th}} + T/2$.

Substituting (12) into (21) and (22) predicts eye closure from the step response. For example, if $T = 100$ ps and $\tau = 25$ ps, the eye closure due to bandwidth-limitation is $s_r(t_s) = 0.88$. The step response reaches 0.98 one period later and the ISI contribution is 0.02. The primary mechanism for eye closure under these conditions is the reduced swing at the sampling time and not bandwidth-limited ISI. The ISI and eye height is plotted in Fig. 6 for the response described by (12) with respect to the 3 dB bandwidth, $1/(2\pi\tau)$, and normalized to bit period. The top plot of Fig. 6 shows the ISI increases as bandwidth decreases. Using (22), the eye closure is plotted in the bottom plot. Significant eye closure (20%) occurs below seven-tenths of the bit rate. The eye closes completely as the bandwidth approaches just above one-tenth of the symbol period.

B. Bandwidth-Limited DDJ

Absolute jitter is the timing deviation from a reference such as the threshold crossing time, t_{th}. The peak DDJ is approximated with a first-order Taylor series using the ISI values at the threshold crossing time [9].

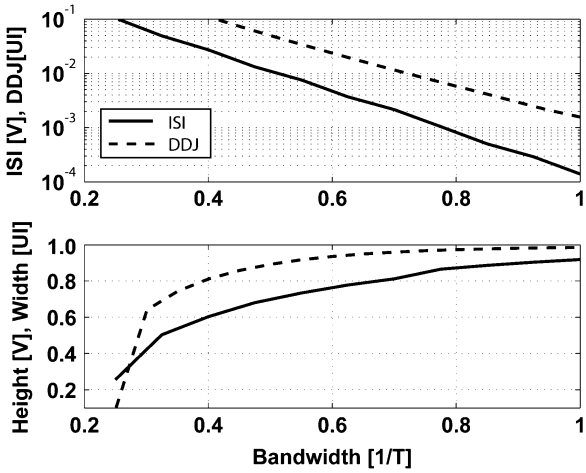

Fig. 6. Bandwidth-limited ISI/DDJ for a cascaded first-order shunt capacitance at the source and load.

$$\mathrm{DDJ}(v_{\mathrm{th}}) = \left| \frac{-\mathrm{ISI}(t_{\mathrm{th}})}{s_r^{(1)}(t_{\mathrm{th}}) + \mathrm{ISI}^{(1)}(t_{\mathrm{th}})} \right|. \tag{23}$$

The superscript denotes the derivative order v_{th}=$s_r(t_{th})$. The DDJ is related to ISI but also depends on slope of the step and ISI. The eye width is the reduction in the symbol period caused by the peak-to-peak DDJ

$$\mathrm{Width}\,(v_{\mathrm{th}}) = 1 - \frac{2}{T}\mathrm{DDJ}(v_{\mathrm{th}}) \tag{24}$$

where the eye width is normalized to the symbol period unit interval (UI). The factor of two in (24) accounts for the peak-to-peak DDJ value.

In Fig. 6, the DDJ and eye width is plotted for the same second-order response from (12) for comparison to the bandwidth-limited ISI. DDJ increases linearly on the log scale as the bandwidth decreases similarly to the behavior of the ISI. While the bandwidth is reduced, the nominal signal slope from (12) at the threshold crossing time is $s_r^{(1)}(t_{\mathrm{th}}) = 3.2/\tau$ and is also reduced. However, the reduction in the eye width is much more gradual than for eye height and remains unaffected until small bandwidths are reached.

C. Echo-Limited Eye Height

The eye height and width in (22) and (24) do not consider reflections but can be modified to include the role of reflections caused by impedance mismatch. The echo ISI is determined from (8) by observing the reflection of prior symbols at the sampling time, t_s, of the current symbol. Since reflections occur over much larger time intervals than the symbol period, an offset time variable accounts for the sampling time, symbol period, and interconnect delay

$$\triangle t_s[k] = t_s - n_k T - 2kT_d \tag{25}$$

where n_k is defined in (6). From this offset time, the ISI from (8) becomes

$$\mathrm{ISI}(t_s) = \max\left\{ \sum_{n=-\infty}^{-1} \triangle a_n \sum_{k=1}^{\infty} v_{r,k}(\triangle t_s[k]) \right\}. \quad (26)$$

The maximum value is taken over all possible combinations for data transition values, $\triangle a_n$. To further simplify this expression, the total echo ISI can be decomposed into an individual ISI contributions from the kth echo

$$\mathrm{ISI}_k(t_s) = \max\left\{ \left| \sum_{n=-\infty}^{n_k} \triangle a_n v_{r,k}(\triangle t_s[k]) \right| \right\} \quad (27)$$

and $\mathrm{ISI}(t_s) = \sum \mathrm{ISI}_k(t_s)$. Since reflections decay with time, the summation includes few symbols after n_k. To illustrate this point, a symbol period of $T = 4\tau$ is superimposed on the first echo at the load in Fig. 5. The reflection lasts over two symbol period and $\triangle a_n$ takes values of 1 and 0 or 1 and -1 since the $\triangle a_n$ sequence must alternate. Subsequent positive and negative values of the reflection accentuate the echo ISI and the difference between the symbol period delayed samples of the reflection contributes to the kth echo ISI. Therefore, the kth echo ISI is simplified from (27) to

$$\mathrm{ISI}_k(t_s) = \max\left\{ \begin{matrix} |v_{r,k}(\triangle t_s[k])|, \\ |v_{r,k}(\triangle t_s[k]) - v_{r,k}(\triangle t_s[k]+T)| \end{matrix} \right\}. \quad (28)$$

If reflections last over more than two symbols, (28) must include more combinations of symbols. On the other hand, if the reflection lasts over one symbol, the ISI depends only on the first term in (28).

The first three echo ISI terms from (28) are plotted as a function of the offset time in Fig. 7 assuming $T = 4\tau$. For example, the worst case ISI contribution from the first echo is $\mathrm{ISI}_1 = 0.13 + 0.5 = 0.18$ and corresponds to the peak height of the first echo ISI term. ISI_1 is maximum for a symbol period of $T = 3.5\tau$ based on the difference between the extrema in (16). Fig. 7 illustrates that ISI_1 introduces the largest possible ISI contribution while the peak ISI for ISI_2 and ISI_3 reaches only 0.07 and 0.05, respectively. However, the ISI_k that makes the greatest contribution total echo ISI depends on the offset time. For instance, at $\triangle t_s[1] = 3\tau$, ISI_1 approaches zero indicating that the first reflection will not impact the overall ISI.

Echo ISI is incorporated into eye closure by modifying (22) to include the echo ISI contributions

$$\mathrm{Height}(t_s[k]) = 2\left[s_r(t_s) - \sum_{k=1}^{\infty} \mathrm{ISI}_k(\triangle t_s[k]) \right] - v_s. \quad (29)$$

Solving the summation involves adding the terms in Fig. 7 at the correct sampling offset times for each echo. Using the echo ISI diagram, the kth echo is sampled at $\triangle t_s[k]$. The offset time is skewed for each echo. To accurately determine the bound in (29), the ISI_k must be added at the correct offset time. The sampling points for each echo ISI term is illustrated graphically in gray in Fig. 7. For the shunt capacitance example from the previous section, the threshold crossing time is defined at $t_{\mathrm{th}} = 1.7\tau$ and, consequently, t_s is located $T/2$ seconds later.

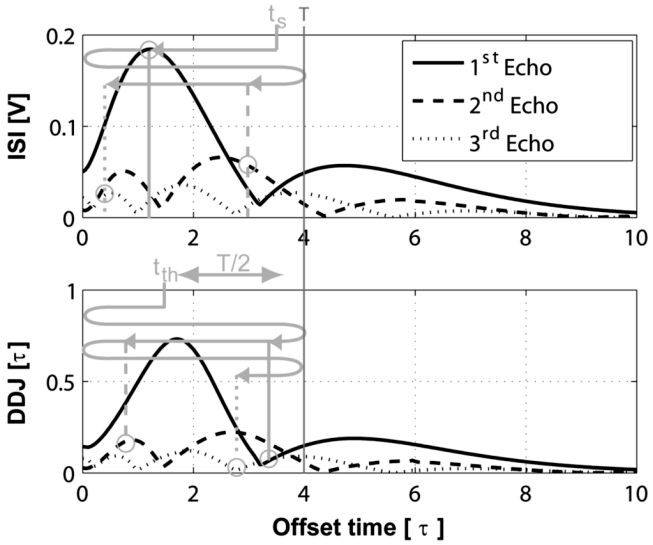

Fig. 7. The worst case contributions to ISI and DDJ from the kth echo at the load for $T = 4\tau$.

The first echo ISI term is sampled at $\mathrm{mod}\{t_s - 2T_d, T\}$, where $\mathrm{mod}\{\}$ is the modulo operator. In the example in Fig. 7, the peak of the first echo ISI contribution is sampled. Subsequent samples wrap around by the interconnect delay modulo the symbol period. The second echo ISI term is sampled at $\mathrm{mod}\{t_s - 4T_d, T\}$. The sampling location of each ISI_k is circled on the diagram. If $2kT_d$ is an integer multiple of T, each echo ISI contribution is sampled at the offset time t_s.

A minimum eye height is estimated from ISI_1. Solving (29) for $k = 1$, the maximum value of 0.18 is possible over all sampling offset times. Substituting $\tau = 25$ ps and $T = 100$ ps, the worst case eye height is $\mathrm{Height}_{\mathrm{wc}} = 2\cdot(0.88 - 0.18) - 1 = 0.4$. Including additional echo terms gives a worst case eye height of $\mathrm{Height}_{\mathrm{wc}} = 2 \cdot (0.88 - (0.18 + 0.06 + 0.02)) - 1 = 0.24$.

A best case eye height is also characterized from the echo ISI terms. The best case eye height is found from the minimum rather than maximum echo ISI contributions from (26) and (27). From the ISI diagram in Fig. 7, the best case eye height is determined from the point where total contribution is minimum and is estimated as $\mathrm{Height}_{\mathrm{bc}} = 2 \cdot (0.88 - 0.075) - 1 = 0.61$. The predicted difference between the worst-case and best-case is the eye height variation and is also an important metric for link implementation. In this case, the eye height variation gives eye closure variation for the channel is 0.37 V. This prediction bounds the eye closure caused by echo ISI.

The eye closure due to echo ISI is plotted in Fig. 8 as a function of the bandwidth of the source and load impedance mismatch. The eye height increases linearly with the bandwidth in contrast to the eye height plot in Fig. 6 for bandwidth-limitation ISI. In effect, less signal energy is reflected for large bandwidths. The eye height is only 0.5 V for wide bandwidths, implying that echo ISI dominates the bandwidth-limited ISI in the absence of attenuation. In this case, echoes cause worst-case eye closure when the bandwidth is 40% of the symbol period. The eye height variation is shown on the right-hand side of the graph. For small bandwidths, the eye remains closed regardless of the best or worst case. Therefore the eye height variation begins at

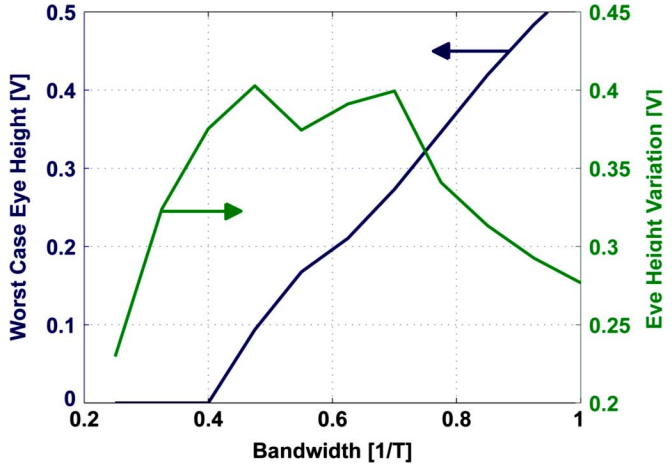

Fig. 8. Reflection-limited eye height for shunt capacitive discontinuities when $T = 4\tau$.

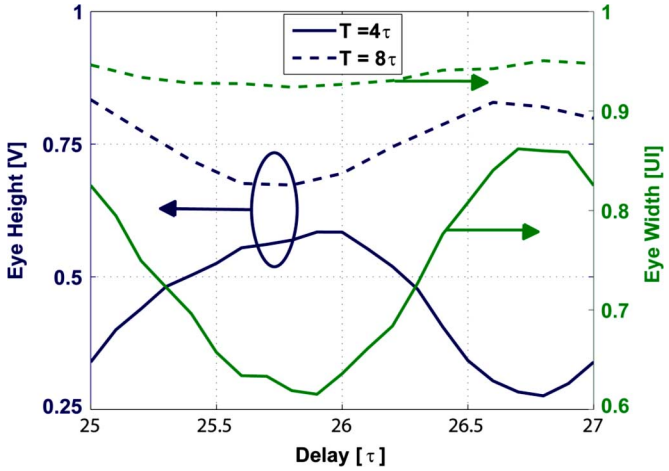

Fig. 9. The eye height and width variation as a function of interconnect delay.

zero. At medium bandwidths, the eye closure variation increases to around 0.4 and remains relatively constant over a range of bandwidths. At larger bandwidth, the difference between the worst and best case eye height reduces and the variation again approaches zero. The eye height variation decreases as the impact of reflections weaken. Therefore, prediction of eye closure due to echoes is most important from the standpoint of signal integrity for bandwidths between 40% and 70% of the symbol period.

D. Echo DDJ

The echo DDJ is also calculated from echo ISI contributions (ISI_k). For DDJ, the derivatives of the reflections effect the signal transition at the threshold crossing time. A worst case peak-to-peak DDJ bound employs the ISI contributions for each echo from (27) evaluated at the threshold crossing time and the step response slope. The peak DDJ from (23) becomes

$$\mathrm{DDJ} \approx \left| \frac{-\sum \mathrm{ISI}_k(\triangle t_{\mathrm{th}}[k])}{s_r^{(1)}(t_{\mathrm{th}}) + \sum \mathrm{ISI}_k^{(1)}(\triangle t_{\mathrm{th}}[k])} \right| \tag{30}$$

where the offset time here relates to the threshold crossing time rather than the sampling time, i.e., $\triangle t_{\mathrm{th}}[k] = t_{\mathrm{th}} - n_k T - kT_d$ and $n_k = \lfloor (t_{\mathrm{th}} - kT_d)/T \rfloor$. At reflection extrema, the derivatives in the denominator are zero and the denominator is the slope of the step response. The worst case DDJ occurs when either the ISI contributions are large or the ISI reduces the transition time. In Fig. 7, the maximum DDJ occurs at a slightly different offset time than the maximum ISI due to the reflection derivatives. To simplify (30), only ISI_1 is considered and the reflection derivative is ignored. Dividing the peak ISI_1 with the slope from the previous section gives a peak DDJ

$$\mathrm{DDJ} \approx 0.18\tau/0.31 = 0.58\tau. \tag{31}$$

The peak-to-peak DDJ is nearly 1.2τ. For $\tau = 25$ ps, this value is roughly 30 ps. When multiple reflections are included, each ISI_k is added DDJ in Fig. 7 following the same approach as for ISI. Summation of these DDJ components is an estimate since the denominator does allow superposition. To calculate the worst case eye width, (31) is combined with (24)

$$\mathrm{Width}(t_{\mathrm{th}}) = 1 - 1.16 \cdot \frac{\tau}{T}. \tag{32}$$

Substituting $\tau = 25$ ps and $T = 100$ ps, the worst case eye width is calculated as 0.71 UI. Equation (32) indicates the eye closure due to jitter for $\mathrm{BW} = 0.18/T$. However, at this bandwidth reflections last over several symbols and cumulatively generate a larger number of deterministic timing deviations.

The eye height and width are subject to variations caused by the symbol period and the interconnect length. Based on the signal integrity in (29) and (32), the interconnect signal integrity as a function of the interconnect delay is predicted. In Fig. 9, the eye closure is plotted as a function of interconnect delay for two symbol periods. The first result is that the higher symbol rate results in reduced eye height and width. The eye height variation in Fig. 9 for $T = 4\tau$ is from 0.63 to 0.26 V for a total of 0.37 V, close to predictions of the previous section. Additionally, the eye width ranges from 0.87 to 0.62 UI for a total variation of 0.25 UI. The eye width was predicted to be 0.71 UI and is near the mean of this range. The second result from Fig. 9 is that the eye height and width variation is much greater for the shorter symbol period as predicted from the eye closure plot in Fig. 8. Finally, the eye height and width are generally inversely related. In effect, the combination of the eye height and width gives an average behavior that is constant with delay.

E. Attenuation

In (10), attenuation was observed to be a factor in the ISI contributions. The previous analysis predicted signal integrity in the absence of attenuation. To include the role of attenuation, (27) becomes

$$\mathrm{ISI}(t_s) = \sum_k e^{-2\alpha kl} \mathrm{ISI}_k(\triangle t_s[k]) \tag{33}$$

where the attenuation is estimated near the 3 dB bandwidth of the impedance mismatch. Since attenuation reduces each echo ISI contribution, the overall impact of attenuation is to reduce

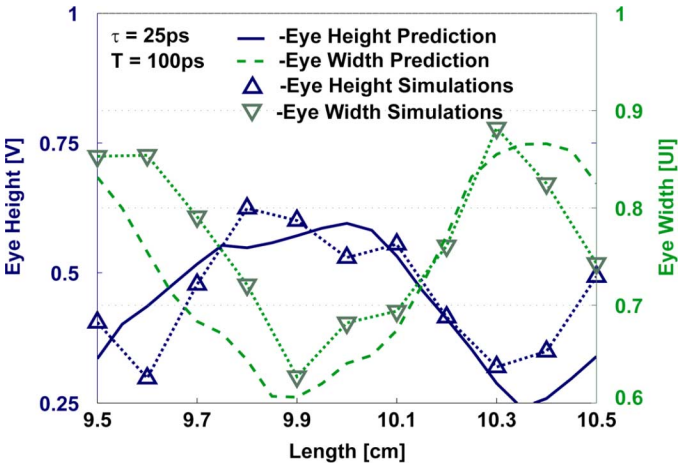

Fig. 10. Simulated eye height and width variation as a function of interconnect length.

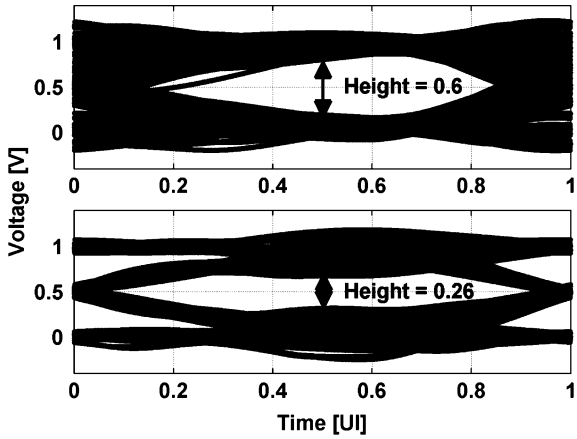

Fig. 11. Eye at the load with no attenuation for maximum eye height (top) and minimum eye height (bottom).

echo ISI. Since reflections have high-frequency energy content, they are more susceptible to frequency-dependent attenuation.

F. Comparison With Full Time Domain Simulations

To verify these predictions, a 2^7-1 PRBS sequence is simulated using Agilent Design System (ADS) and the eye height and width are plotted in Fig. 10 as a function of length and compared to the predictions in Fig. 9. ADS is a comprehensive tool for simulating interconnect performance because the compatibility between time-domain models and frequency domain models based on high-frequency SPICE or full-wave electromagnetic field solvers (Momentum) provides the ability to fully model the interconnect environment.[1] The source and load for this simulation are 50 Ω terminations in parallel with 1 pF shunt capacitance. Each simulation is carried out over 12.7 ns with 200 fs timing resolution. The interconnect model is an ideal transmission line of nominal length of 10 cm. No attenuation is modeled to provide worst-case comparison with the predictions. The eye diagram is simulated at 0.1 cm intervals and the eye closure is plotted in Fig. 10. The maximum and minimum values for the eye height and width of the simulations agree with the predictions. Fig. 10 shows that the simulated worst case eye opening was 0.3 V while the prediction was 0.24 V, an error of 20%. Similarly, the eye width is simulated as 65 ps. The worst-case jitter prediction was 71 ps giving an error of around 10%. The best case eye height and width are 0.75 and 88 ps. Data eyes corresponding to the best case and worst case eye height, corresponding to a length of 9.8 cm, and width, corresponding to a length of 10.3 cm, are plotted in Fig. 11 at 10 Gb/s. In the top data eye, the eye height is maximum at the expense of the DDJ. In the bottom data eye, the eye width is maximum at the expense of ISI. The predicted eye height and width matched the results of a full time domain simulation with a PRBS stimulus. The advantage of the prediction calculation is that it can bypass computationally intensive time-domain and frequency-domain simulations over a large range of interconnect parameters and identify worst-case behavior more quickly.

[1]http://eesof.tm.agilent.com/products/design_flows/signal_integrity/

VI. Passive Equalization

Bandwidth limitations of the interconnect cause eye closure at high data rates. NRZ signaling rates are improved only with equalization techniques such as finite-impulse response (FIR) filtering or nonlinear techniques such as decision feedback equalization (DFE). Limited bandwidth causes ISI from neighboring symbols while echo ISI poses a broader problem since the current symbol contains ISI over larger time spans [6], [8]. While digital equalization techniques offer adaptability over a range of channel environments, they tend to consume more power [18]. Alternatively, passive equalizers are generally two-port matching networks constructed from passive elements at the transmitter or receiver to improve the link performance. Consequently, recent work has explored these implementations for maximizing performance of chip-to-chip interconnects [22]–[25]. Passive equalizers offer limited adaptation but consume little power, allowing the lowest energy consumption as measured in picojoules per bit. Passive equalizers may be implemented on-chip or through a combination of board-package-chip co-design. However, the equalizer network may result in higher return loss and more signal reflection. Predicting signal integrity for passive equalizers is particularly pertinent since the reconfigurability is limited. A one-port passive equalizer is illustrated in Fig. 12 [24]. This equalizer can be implemented at the transmitter or receiver. For broadband performance, the one-port network provides a termination impedance of

$$Z_{ol} = sL_t + R_t. \tag{34}$$

The termination impedance increases to compensate the shunt capacitance. The inductance creates peaking near $\omega_p = 1/\sqrt{L_t C_s}$. Approaches to designing the passive equalizer include extending the 3 dB bandwidth or flattening group delay. Here, the signal integrity algorithm demonstrates an appropriate choice of the peaking frequency subject to maximization of the eye height and width.

Source and load reflections are caused by the parallel combination of the load impedance in (34) with the shunt capacitance and are calculated by substituting this impedance into (19) and

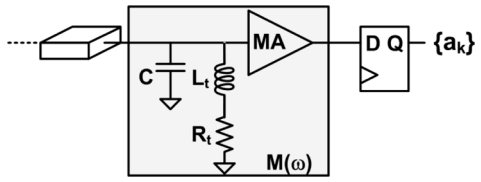

Fig. 12. One-port passive equalization.

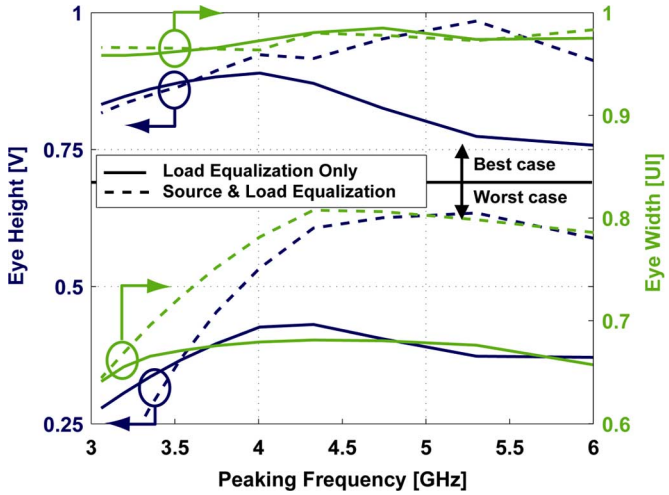

Fig. 13. Predicted eye height and width as a function of series peaking frequency.

(20). The resulting reflection coefficient is applied to the algorithm developed in Section V to determine the eye height and width. The shunt capacitance is assumed to be 1 pF and the symbol period is 100 ps. In Fig. 13, the performance of passive equalization is analyzed when implemented only at the load or at both the source and load, where the equalizers are assumed to be identical. The best and worst case eye height and width are illustrated as a function of the choice of peaking frequency.

As the inductance increases, the peaking frequency is reduced. Under both implementations, the best and worst case eye height increases, reaches a maximum value, and decreases when the peaking results in excessive ringing. However, the optimal peaking frequency depends on which implementation is used. The combination of source and load equalization achieves superior best case and worst case eye height compared to the load equalizer. The eye height is as much as 0.2 V larger and the eye width is as much as 0.2 UI larger when compared with equalization at the load alone. For the source and load equalizer, the peaking frequency is located at around 5 GHz or roughly 85% of the 3 dB frequency. While the worst case eye width follows the worst case eye height, the best case eye width is relatively insensitive to the choice of peaking frequency. In both scenarios, the eye height and width variation remain constant with the choice of peaking frequency until the best case eye height and width reduces.

To verify these predictions, the combination of source and load equalization is simulated in ADS using the same approach described in Section V over a range of interconnect lengths with a termination inductance of $L_t = 1$ nH and $R_t = 50\ \Omega$ for a $2^7 - 1$ PRBS sequence. The results are plotted in Fig. 14 and

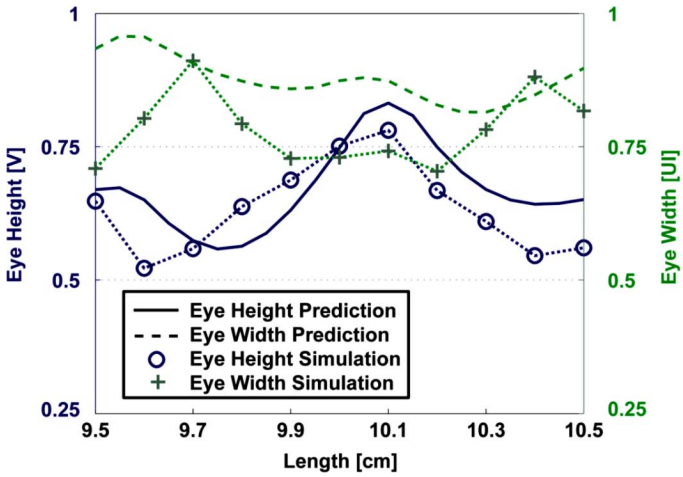

Fig. 14. Simulated eye height and width for passive equalization at the source and the load.

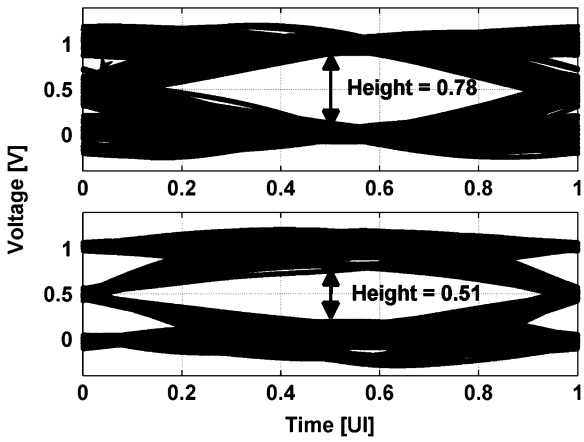

Fig. 15. Data eye for maximum eye height (top) and minimum eye height (bottom) with passive equalization network at the transmitter and receiver.

compared with eye height (solid line) and width (dashed line) predictions of the interconnect signal integrity based on a single reflection. When compared to the eye closure without equalization in Fig. 10, the best and worst case eye height is improved by about 0.18 V with passive equalization while the variation in the signal integrity remains about the same. At the same time, the worst-case eye width does not change dramatically but the minimum eye width increases by about 0.05–0.1 UI.

Finally, the data eye is provided for the interconnect length that provides the best and worst case eye opening from Fig. 15. Since shunt capacitance of the transmitter and receiver is identical to the situation in Fig. 11, the data eyes are compared to illustrate the eye closure improvement due to the passive equalizer. For the best case, the eye height was increased from 0.6 to 0.78 V or an improvement of 0.18 V. For the worst case, the eye height increased from 0.26 to 0.51 V or an improvement of 0.25 V. While this analysis is applied to a one-port equalizer, more general passive equalizer networks could be analyzed in a similar manner. Passive equalizers allow extension of the 3 dB bandwidth of the serial link. More importantly, the link performance is only improved by increasing the eye height and width and the impact of reflections can be studied using this technique.

VII. Conclusion

A method for predicting signal integrity identifies the relationship between signal echoes and the interconnect impedance mismatch, symbol period, and interconnect delay. The advantage of this method is that interconnect eye height and width are assessed quickly without extensive time domain simulation over all parameters. This paper examines the fundamental trade-off between bandwidth and return loss. For linear channels, the impact of impedance mismatch is separated into components affecting the step response (bandwidth-limited ISI) and generating echoes (reflection-limited ISI). The relationship between echoes and signal integrity in serial links is derived and an analysis for predicting best and worst case signal integrity is described. Bounds on the intersymbol interference and data-dependent jitter are constructed for capacitive discontinuities and compared to simulation results. Finally, this predictive signal integrity technique is applied to the design of a passive equalizer to show the optimal choice of peaking inductance for eye closure.

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